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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/524,408	CHAKRABORTY ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Final Action

Introduction

1. Title is: METHOD AND APPARATUS FOR APPLYING FINE GRAINED TRANSFORMS DURING PLACEMENT SYNTHESIS INTERACTION
2. First named inventor is: CHAKRABORTY
3. Claims 1-39 have been submitted, examined, and rejected.
4. The independent claims are: 1, 16, 21, 22, 37-39.
5. This action is in reply to Applicant's Amendment filed 12/23/03, which amends claims 1, 3, 5, 11, 13, 16, 17-22, 24, 26, 34, 37-39, and purports to amends FIG 2, 3, and 7.
6. Amendment page 11 discusses amendments to drawings, FIG 2, 3, and 7. However, no amended drawings have been submitted.
7. US Application was filed 03/13/00, and there are no claims for earlier priority.

Index of Prior Art

8. **Shenoy** refers to US Patent 6,378,114.

Applicant's Remarks

9. Applicant's Remarks, pages 12-17, are addressed in the order presented by Applicant, with subheadings added by the Examiner for clarity.
10. 35 USC 112, FIRST PARAGRAPH, INTERACTIVE AXES, SIMULTANEOUS. The Applicant concedes the three domains (Boolean, electrical, and physical) are interrelated, and "Applicants do not contend that Figure 1 accurately illustrates all performances of the traditional methods". Applicant traverses the prior action's statement that changes to a single domain must be propagated sequentially to the other domains. However, Applicant does not present any persuasive assertion that the changes may be optimized simultaneously.
11. Applicant does persuasively assert that the invention evaluates "the effects of any change in all three domains". However, said changes appear to be propagated sequentially, and not simultaneously.
12. MULTIPLE CRITERIA OPTIMIZATION. However, it is not accurate to state that "Applicants' invention assures that various metrics are optimized concurrently with the application of any single optimization", Remarks page 14. The integrated circuit design process may accurately be described as a multiple criteria (factor) optimization problem, see

Shenoy column 1 line 66 "overall design". Unfortunately, typically it is impossible to simultaneously optimize each of the individual multiple criteria. For example, larger gates (or additional buffers) will speed the signal processing (good), but larger gates will also take more space and consume more power (bad). In simple systems, an objective "overall" function is defined to represent the quality of the system design (for example, a sum of appropriately weighted individual factors), and said objective function may be optimized (within any given constraints).

13. Applicant's invention does not define any such objective function. Rather, Applicant's invention appears to make a single change in a first domain, then propagates said change sequentially into the other domains, then possibly checks whether any of said other domains violate given constraints. Thus, it is not accurate to state that Applicants' invention "assures that various metrics are optimized concurrently with the application of any single optimization", at Remarks page 14.
14. CONVERGE. Applicant asserts that "converge" is a recognized term, citing Shenoy column 3, line 52. However, Shenoy states "a determination is made as to whether the current placement has successfully converged. Convergence is achieved when each of the partitions reaches a pre-determined size. For example, the user can set the convergence point to occur when each of the partitions is comprised of less than twenty gates." Thus, Shenoy defines convergence for partitioning during placement, and placement would a portion of Applicant's "physical" domain (including "layout area... congestion" at Remarks page 12). Shenoy does not define convergence for an objective criteria function for three interrelated domains (Boolean, electrical, and physical).
15. 35 USC 112, SECOND PARAGRAPH, MORE AND LESS GRANULAR. Applicant has removed the term "more and less" from the original claim 1, and replaced it with the term "less-to-more granular". Applicant Remarks states "That is, a set of placements and netlist transforms are being provided which at one end of the set are less granular and at the other end of the set are more granular". However, it is still not clear what Applicant intends by "less granular" and "more granular" placements and transforms.
16. DECOMPOSED. Applicant defines the term "decomposed" as "division of a larger item into a series of smaller items", citing Shenoy column 1 lines 18-20 which states "computers can

be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions". The Examiner adopts this definition.

17. SELECTIVELY MIXED AND MATCHED WITH PREDETERMINED LOGIC SYNTHESIS TRANSFORMS AND FINE-GRAINED TRANSFORMS. The Applicant states "once a large step is divided into a set of smaller (fine-grained) transformations, a combinations of the smaller steps may be used in varuous permutations and combinations based on the optimization required".
18. SELECTIVELY OPTIMIZES. This term is moot due to deletion by amendment.
19. FINE-GRAINED TRANSFORMS ARE ORGANIZED TOGETHER IN FLEXIBLE SCENARIOS TO CREATE A DESIGN CLOSURE PROCESS. Applicant defines the term "scenario" as a sequence of transformations.
20. INTERCEPT A PROCESS. Applicant asserts that, in a "scenario", a different set of transformation may be selected by a conditional operator based upon the state of the design. The Examiner adopts this definition for "intercept a process" in a scenario.
21. UNIFIED VIEW. Applicant defines "unified view" as "common database repository and application programming interface for all data regarding the design - - Boolean, electrical, and physical".
22. 35 USC 102 (e), TWEAKED TO OPTIMIZE. Applicant asserts that Shenoy does not disclose what might be done to "tweak" the netlist. However, Shenoy clearly discloses the sequential design process (column 1 "define the performance specification... translate into functional criteria... generates a netlist... place and route... specific layout"), and clearly discloses the iterative nature of circuit design (column 1 "Often, several iterations of the design, layout, and testing process are required in order to optimize the semiconductor chip's size, heat output, speed, power consumption, and electrical functionalities"), and discloses the complex interrelationships (column 1 "high degree of interdependence makes it extremely difficult to predict and account for the consequences associated with any changes. Indeed, the overall design might sometimes be worse in a successive iteration"). Thus, one of ordinary skill in the art would interpret Shenoy's column 3 "netlist is tweaked to optimize the desing" as disclosing modifications which would affect the chip's size, heat output, speed, power consumption and electrical functionalities. Shenoy column 3 explicitly cites

one example of tweaking: "buffers may be added to increase the speed... may cause the area to increase". Note that reasonable "inferences", and "common sense" may be considered in formulating rejections for obviousness. Specifically, *In re Preda*, 401 F.2d 825, 159 USPQ 342, 344 (CCPA 1968) states "in considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." Also, *In re Bozek*, 416 F.2d 738, 163 USPQ 545, 549 (CCPA 1969) states that obviousness may be concluded from "common knowledge and common sense of the person of ordinary skill in the art without any specific hint or suggestion in a particular reference". Additionally, see *In re Gauerke*, 24 CCPA 725, 86 F.2d 330, 31 USPQ 330, 333 (CCPA 1936), and *In re Libby*, 45 CCPA 944, 255 F.2d 412, 118 USPQ 94, 96 (CCPA 1958), and *In re Jacoby*, 309 F.2d 738, 125 USPQ 317, 319 (CCPA 1962), and *In re Wiggins*, 488 F.2d 538, 543, 1979 USPQ 421, 424 (CCPA 1973).

23. ALL THREE DOMAINS, CONCURRENTLY. Applicant asserts that the claimed invention considers all three domains (Boolean, electrical, and physical) concurrently. However, Shenoy column 1 clearly discloses propagating modifications downstream to the other domains, and considering the overall result ("a minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages... extremely difficult to predict... Indeed, the overall design might sometimes be worse in a successive iteration"). Thus, the Examiner agrees that the overall design may be judged in view of all three domains, however, changes in one domain propagate sequentially to the other domains, and all three domains cannot be optimized "concurrently".
24. CLAIM AMENDMENTS. The amended claims are considered in the similarly amended rejections below.

Specification and Drawings

25. A discussion of the specification and drawings is useful as a support for the 35 USC 112 rejections, because most of the enablement and indefinite rejections spring from a common theme. The common theme is simultaneous optimization of multiple domains, which is repeatedly claimed with slightly varying terminology. It appears efficient to discuss

simultaneous optimization in detail now, rather than repeating the entire discussion for each 35 USC 112 rejection.

26. THREE SEPARATE DOMAINS. Applicant presents an interesting broad conceptual approach to integrated circuit design, whereby the circuit design space is defined by three separate domains, "in Figure 1, the three axes represent optimizations along Boolean, electrical and physical domains" at specification page 5 lines 3-4. Said broad conceptual approach is useful for broad conceptual or theoretical discussions.
27. However, Applicant's representation of circuit design space is a bit simplistic in a practical sense, because the three domains interact in a complex, non-linear, and unpredictable fashion. See Shenoy Column 1. Optimizing in one domain generally degrades another domain. For example, circuit elements (transistors) with larger areas are faster (electrical domain), but take more layout area (physical domain). Thus, Applicant's representation of the prior art's sequential optimization as traveling sequentially from point to point in directions parallel with the axes (specification page 5 and FIG 1 points A-F) is not fully accurate because the axes are interactive.
28. Note that optimization in a single domain will simultaneously affect the other domains. For example, the electrical and physical domains are directly related, as discussed in the transistor example above. The Boolean domain is slightly different because the electrical and physical domains may be changed without changing the Boolean domain. However, any change in the Boolean domain will always change both the physical and electrical domains. See Shenoy column 1.
29. Further, at specification page 9 line 17, Applicant asserts that "a single step may optimize the physical, Boolean and electrical dimensions, thus moving the design from point A to F' in the design space. Multiple steps are not required". This broad assertion is not supported. For example, first the Boolean space is changed, then this change is propagated to the electrical domain (new electrical elements to implement the new Boolean logic, and new basic characteristics of the new electrical elements), and then propagated to the physical (layout) domain, and then propagated to the electrical domain again (capacitance of connecting lines, noise from connecting lines, and related electrical characteristics that are dependent upon the layout of the electrical elements). See Shenoy column 1. **This simple**

example illustrates the point that changes to a single domain must be propagated sequentially to the other domains, and that the "overall design" (Shenoy column 1 line 66) is optimized, and all three domains are not optimized simultaneously. See above Remarks section discussing objective function multiple criteria optimization.

30. Thus, "simultaneous" (claim 1 (amended) preamble) optimization in multiple domains is repeatedly claimed, but is not adequately supported by the specification. See above related discussion in Applicants' Remarks section.
31. COMPLEXITY OF INTEGRATED CIRUITS. Modern integrated circuits are probably the most complex creations of man. They contain millions of individual electrical elements, tightly packed into three dimensions, with electric charges generating electric fields, and with moving charges generating magnetic fields, with heat being generated and dissipated, with logical operations occurring, and with all of these chemical, electrical, logical, quantum semiconductor, and thermal phenomenon interacting in space and in time at frequencies of millions or billions of cycles per second. Thus, the design of integrated circuits is highly unpredictable. See the Wands 8 factor test regarding undue experimentation, particularly factor (7) "the predictability or unpredictability of the art", *In re Wands* (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998).

35 USC § 101-statutory subject matter

32. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful **process, machine, manufacture, or composition of matter,** or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.
33. **Claim 22-39 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter,
34. Independent claim 22 (amended) preamble states "A system for applying transforms for modifying a plurality of domains concurrently in a design space, said method comprising:" Thus, the preamble appears to claim "system" and "method" simultaneously, and it appears that "system" is intended as the "machine" statutory category, and "method" is intended as the "process" statutory category. Further, note the three limitations state "a unit for... a unit to...", and thus appear intended as "machine" statutory category limitations. Thus, multiple statutory classes are improperly claimed.

35. See MPEP 2173.05(p)(II), which states:

> A single claim which claims both an apparatus and the method steps of using the apparatus is indefinite under 35 U.S.C. 112, second paragraph. In Ex parte Lyell, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990), a claim directed to an automatic transmission workstand and the method steps of using it was held to be ambiguous and properly rejected under 35 U.S.C. 112, second paragraph.
>
> Such claims should also be rejected under 35 U.S.C. 101 based on the theory that the claim is directed to neither a "process" nor a "machine," but rather embraces or overlaps two different statutory classes of invention set forth in 35 U.S.C. 101 which is drafted so as to set forth the statutory classes of invention in the alternative only. Id. at 1551.

36. Claims 23-36 depend from claim 22, and are rejected for the same reasons.

37. Claim 37 (amended) states "a software system" with "modules", and software is not a statutory class. See MPEP 2106 regarding computer related inventions.

38. Claim 38 (amended) and 39 (amended) state "programmable storage medium... said method comprising". Thus, it appears that the statutory classes "manufacture" (article of manufacture) and "process" are improperly simultaneously claimed.

35 USC § 112- first paragraph- enablement

39. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

40. **Claims 1-39** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

41. Claims 1 (amended) states **"selectively applying a set of less-to-more granular placement and netlist modification transforms".** Applicant has removed the term "more and less" from the original claim 1, and replaced it with the term "less-to more granular". Applicant Remarks states "That is, a set of placements and netlist transforms are being provided which at one end of the set are less granular and at the other end of the set are more granular". However, it is still not clear what Applicant intends by "less granular" and "more granular"

placements and transforms. The specification does not adequately describe the term "less-to-more granular". Specification page 6 line 8 states "single fined-grained step which may comprise of multiple objectives and constraints which involve both physical (placement), electrical and logical data". Further, specification page 16 line 22 states "a fine-grained transform unit 308 for placing sizeless cells which have only gain values assigned to them". Also, specification page 14 line 11 states "bins... hold logic and a rough (course) representation of where the chip is (or should be located)".

42. Additionally, claim 1 (amended) states **"simultaneously modifying a plurality of domains".** Said "simultaneously" modification is not enabled, see discussion in Remarks section above, because the modifications are propagated sequentially to the domains. See Shenoy column 1.
43. Claims 2-15 depend from claim 1, and are rejected for the same reasons.
44. Claim 5 (amended) states **"a single transform optimizes the physical, Boolean and electrical domains",** and is not enabled for the same reasons as claim 1. Additionally, Shenoy column 1 clearly discloses propagating modifications sequentially downstream to the other domains, and considering the overall result ("a minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages... extremely difficult to predict... Indeed, the overall design might sometimes be worse in a successive iteration"). Thus, it is not clear how a single transform can optimize all domains simultaneously.
45. Claim 9 states **"utilizing an infrastructure of bins, and wherein a timing, congestion and noise analysis is based on the bins".** Congestion analysis based upon bins is enabled, but the specification does not enable timing and noise analysis based upon the bins. Note that timing requires the netlist and the electrical properties of the elements, and cannot be analyzed based upon the bins. Further, the exact wiring layout also affects capacitance, and thus affects the timing. Similarly, the noise cannot be analyzed based upon the bins. However, the congestion could be analyzed based upon the bin area utilization.
46. Claim 10 states **"placement and netlist changes are performed together in said fine-grained transforms",** and is not enabled for the same reasons as claim 1.

47. Claim 15 states "synthesis, timing, and placement data are concurrently available to all of said transforms, such that said **transforms modify a netlist and placement concurrently**", and is not enabled for the same reasons as claim 1.
48. Claim 16 (amended) states **"applying transforms the change the physical, electrical and Boolean logic design space concurrently",** and is not enabled for the same reasons as claim 1.
49. Claims 17-20 depend from claim 16, and are rejected for the same reasons.
50. Claim 17 (amended) states **"design convergence".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. The specification does not enable simultaneous convergence in the three domains. See Shenoy column 1 line 66 "Indeed, the overall design might sometimes be worse in a successive iteration".
51. Claim 18 (amended) states "considering concurrently subsets of fine-grained Boolean transforms, electrical transforms, and physical transforms", and is not enabled for the same reasons as claim 1.
52. Claim 19 (amended) states **"the transforms are interspersed sequentially".** It is not clear how transforms can be considered "concurrently" in parent claim 18 (amended), and then "sequentially" in claim 19 (amended).
53. Claim 21 (amended) states **"applying transforms that change the physical, electrical and Boolean space concurrently... until design convergence",** and is not enabled for the same reasons as claim 1 and claim 17.
54. Claim 22 (amended) is rejected as not enabled for the same reasons as claim 1 (amended).
55. Claims 23-36 depend from claim 22, and are rejected for the same reasons.
56. Claims 26, 30-31, and 36 are "system" claims with the same limitations as "method" claims 5, 9-10, and 15 respectively, and thus are not enabled for the same reasons respectively.
57. Claim 37 (amended) states **"modifying a plurality of domains concurrently",** and is not enabled for the same reasons as claim 1 (amended).
58. Claim 38 (amended) states **"converging design flow process... optimize... concurrently",** and is not enabled for the same reasons as claim 1 (amended).

59. Claim 39 (amended) states **"transforms that change the physical, electrical and Boolean space concurrently",** and is not enabled for the same reasons as claim 1 (amended).

35 USC § 112-Second Paragraph-indefinite claims

60. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

61. Claims 1-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

62. Claim 1 (amended) states **"selectively applying a set of less-to-more granular placement and netlist modification transforms".** Applicant has removed the term "more and less" from the original claim 1, and replaced it with the term "less-to more granular". Applicant Remarks states "That is, a set of placements and netlist transforms are being provided which at one end of the set are less granular and at the other end of the set are more granular". However, it is still not clear what Applicant intends by "less granular" and "more granular" placements and transforms. The specification does not adequately describe the term "less-to-more granular". Specification page 6 line 8 states "single fined-grained step which may comprise of multiple objectives and constraints which involve both physical (placement), electrical and logical data". Further, specification page 16 line 22 states "a fine-grained transform unit 308 for placing sizeless cells which have only gain values assigned to them". Also, specification page 14 line 11 states "bins... hold logic and a rough (course) representation of where the chip is (or should be located)".

63. Similarly, claims 1, 3, 4, 6, 16, 21, 37, 38, 39 state **"fine-grained",** which is not adequately defined. Note that specification page 16 refers to "sizeless cells", but page 6 refers to "physical (placement)". Again, these specification sections appear contradictory.

64. Claim 3 (amended) states **"said placement and netlist modification transforms are decomposed into a set of fine-grained transforms each addressing a specific phase of the placement and synthesis process".** Applicant defines the term "decomposed" as "division of a larger item into a series of smaller items", citing Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits

into a multitude of simpler functions". The Examiner adopts this definition. However, it is not clear how "transforms" can be decomposed into "fine-grained transforms". Rather, in the context of Shenoy, the term "transforms" appears to refer to the sequential stages (transformations) of the design process discussed at column 1 lines 26-40: "define the performance specification... translate this specification into functional criteria... fed into a logic synthesis program... generates a netlist...". It appears that the overall design process consists of a discrete series of transformations, and it is not clear what the Applicant intends by decomposing transforms. Shenoy uses the term "decompose" regarding breaking a large complicated circuit into simpler functions.

65. Claim 5 (amended) states **"a single transform optimizes the physical, Boolean and electrical domains",** and is not enabled for the same reasons as claim 1. Additionally, Shenoy column 1 clearly discloses propagating modifications sequentially downstream to the other domains, and considering the overall result ("a minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages... extremely difficult to predict... Indeed, the overall design might sometimes be worse in a successive iteration"). Thus, it is not clear how a single transform can optimize all domains simultaneously. Note the term "simultaneously" in the preamble of claim 1, which is the base claim of claim 5.
66. Claim 6 states "**a single fine-grained transform** includes multiple objectives and constraints which involve physical placement and logical data. It is not clear how a single transform can include multiple objectives and constraints involving both physical placement and logical data.
67. Claim 8 states **"a single converging flow of fine grained operations".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. It is not clear what "convergence" means with respect to optimizing the three domains.
68. Claim 13 (amended) states "**examining a plurality of domains concurrently in finding an optimum design, said examining comprising creating a sequence of less-to-more**

granular placement and netlist transforms, to create a converging design closure process". Claim 13 is indefinite for the same reasons as claim 1.

69. Claim 16 (amended) states **"applying transforms the change the physical, electrical and Boolean logic design space concurrently"**, and is indefinite for the same reasons as claim 1.
70. Claims 17-20 depend from claim 16, and are indefinite for the same reasons.
71. Claim 17 states **"design convergence is achieved".** Webster defines "converge" as "to tend or move toward one point or another... to approach a limit". As previously discussed, the physical, electrical and Boolean logic design domains have complex, non-linear, and unpredictable relationships. It is not clear what "convergence" means with respect to optimizing the three domains. See above discussion in Remarks section regarding "simultaneous" and "converge" and "concurrently".
72. Claim 18 (amended) states **"design space is moved from one point to another by considering concurrently subsets of fine-grained Boolean transforms, electrical transforms, and physical transforms".** It is not clear how said transforms can be considered "concurrently", when it appears that they must be applied sequentially.
73. Claim 19 (amended) states **"the transforms are interspersed sequentially".** It is not clear how transforms can be considered "concurrently" in parent claim 18 (amended), and then "sequentially" in claim 19 (amended).
74. Claim 20 (amended) states **"each of said transforms is represented as a plurality of transformations such that the optimizations are divided and interspersed sequentially, to examine each of the Boolean, electrical and physical domains concurrently".** Claim 20 (amended) is indefinite for the same reasons as claim 19 (amended).
75. Claim 21 (amended) is rejected for the same reasons as claim 17.
76. Claims 22-36 are rejected as indefinite for the same reasons as claims 1-15 respectively.
77. Claim 37 (amended) states **"modifying a plurality of domains concurrently"**, and is indefinite for the same reasons as claim 1 (amended).
78. Claim 38 (amended) states **"converging design flow process... optimize... concurrently"**, and is indefinite for the same reasons as claim 1 (amended).
79. Claim 39 (amended) states **"transforms that change the physical, electrical and Boolean space concurrently"**, and is indefinite for the same reasons as claim 1 (amended).

80. Claims 22-39 are further rejected as indefinite for simultaneously claiming multiple 35 USC 101 statutory classes, as discussed above.

35 USC § 102(e): filed before 11/29/00 and not vol. pub. under 35 USD 122(b)

81. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

82. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

83. **Claims 1-15, and 22-37 are rejected under 35 U.S.C. 102(e)** as anticipated by Shenoy US Patent 6,378,114.

84. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.

85. Claim 1 is an independent "method" claim with 5 limitations, labeled by the Examiner for clarity.

86. [1] **"selectively applying a set of less-to-more granular placement and netlist modification transforms separately or in a flexible sequence to create a converging design process flow"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

87. [2] **"evaluating the impact of the set of modification transforms on the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

88. [3] **"rejecting evaluated transforms that do not improve the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
89. [4] **"repeating the above to create a converging design process flow"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
90. [5] **"wherein said transforms comprise fine-grained steps to optimize the netlist and placement properties of a design"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
91. Claims 2-15 depend from claim 1, and are rejected below.
92. In claim 2, **"said creating starts from a netlist without an initial placement of said circuit or from a netlist with an initial placement"** is disclosed by Shenoy at column 1 line 31 "the synthesis program generates a netlist... Next, a physical design tool is used".
93. In claim 3 (amended), **"said placement and netlist modification transforms are decomposed into a set of fine-grained transforms each addressing a specific phase of the placement and synthesis process"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions". Applicant Remarks defines the term "decomposed" as "division of a larger item into a series of smaller items".
94. In claim 4, **"said placement transforms are selectively mixed and matched with predetermined logic synthesis transforms and fine-grained transforms"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions", and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the

results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

95. In claim 5 (amended), **"a single transform optimizes the physical, Boolean and electrical domain, thus moving the design from a start point to an end point in the design space"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions", and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
96. In claim 6, **"a single fine-grained transform includes multiple objectives and constraints which involve physical placement and logical data"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions", and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
97. In claim 7, **"a partially placed and synthesized design is a starting point of said creating"** is disclosed by Shenoy at column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design" and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".
98. In claim 8, **"said process flow comprises a single converging flow of successive application of fine-grained operations"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

99. In claim 9, **"utilizing an infrastructure of bins, and wherein a timing congestion and noise analysis is based on the bins"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

100. In claim 10, **"placement and netlist changes are performed together in said fin-grained transforms"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

101. In claim 11 (amended), **"fine-grained transforms are organized together in flexible scenarios to achieve a design closure process"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

102. In claim 12, **"at predetermined stages of the process, selectively determining whether to intercept the process and implement any of a plurality of fine-grained transforms"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

103. In claim 13 (amended), **"examining a plurality of domains concurrently in finding an optimum design, said examining comprising creating a sequence of less-to-more granular placement and netlist modification transforms, to create a converging design closure process"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

104. In claim 14, **"all transforms have a unified view of the placement and synthesis design space"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions". Applicant Remarks defines "unified view" as "common database repository and application programming interface for all data regarding the design - - Boolean, electrical, and physical". One of ordinary skill in the art would interpret Shenoy's "computers" as disclosing a common database for all data regarding the design, because using a common database simplifies performing the requisite iterative design steps.

105. In claim 15, **"synthesis timing, and placement data are all concurrently available to said transforms, such that said transforms modify a netlist and placement concurrently"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

106. Claim 22 (amended) is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.

107. Claim 22 (amended) is an independent "method" claim with 3 limitations, labeled by the Examiner for clarity.

108. [1] **"creating a sequence of less-to-more granular placement and netlist modification transforms"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

109. [2] **"evaluate the impact of the sequence of modifications transforms on the design space and to reject evaluated transforms that do not improve the design space to create a converging design process flow"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

110. [3] **"said transforms are fine-grained transforms allowing selective mixing and matching of said fine-grained transforms to optimize the placement of a circuit in a design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

111. Claims 23-36 depend from claim 22, with the same additional limitations as claims 2-15, and are rejected for the same reasons.

112. Claim 37 (amended) is an independent "software system" claim, with the same limitations as "method" claim 22 (amended), and is rejected for the same reasons.

Response to Amendments or new IDS-FINAL OFFICE ACTION

113. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusions

114. All claims 1-39 stand rejected. Most claims stand rejected for multiple reasons.

115. As a procedural suggestion, the Applicant may find it efficient to adopt the classic 35 USC 101 statutory class nomenclature ("process, machine, manufacture, or composition of matter, or any new and useful improvement thereof") in the claims. The use of other nomenclature (particularly the vague term "system") tends to obscure the intended statutory class, and tends to cause 35 USC 101 rejections.

116. Amendment page 11 discusses amendments to drawings, FIG 2, 3, and 7. However, no amended drawings have been submitted.

Communication

117. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 7:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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